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## Reversible computing for digital circuits

In recent years, reversible computing is mostly used to propose digital circuits which make use of reversible logic gates. These gates are mainly used to enhance the effectiveness of digital circuits by mitigating the power utilization, quantum cost, number of constant inputs, number of garbage outputs etc. A variety of combinational plus sequential digital circuits have been prepared efficient by means of these reversible logic gates. This article gives a concise introduction to reversible computing and also work done by different authors in previous years has been studied.

In 1961, R.Landauer [1] stated that in irreversible logic computation heat dissipates due to Loss of information bits. Each bit of information dissipates  $kT\ln 2$  amount of heat, where  $k$  is the Boltzmann constant and  $T$  is the absolute temperature. In 1973, C.H.Bennett [2] stated that this heat dissipation problem can be solved by using reversible computation. Reversible computing follows the property of reversibility in which there is one to one mapping between the input and output vectors. A circuit is set to be reversible if the input vectors can be distinctively retrieved from the output vectors

### Basic Definition and Parameters of Reversible Logic Gates

A reversible logic gate has  $n$  inputs and  $n$  outputs with one-to-one correspondence. Fan out is not allowed in reversible circuits. There are many parameters for determining the performance of reversible circuits.

1. Number of Reversible gates (N): It refers to the number of Reversible gates used in the circuit.
2. Number of Constant outputs (CI): It refers to the number of inputs that need to be maintained constant at either 0 or 1.
3. Number of garbage outputs (GO): It refers to the number of idle outputs represented in reversible logic circuit.
4. Quantum cost (QC): This refers to the cost of circuit in terms of primitive gate.

### Basic Reversible Logic Gates

1) NOT Gate The simplest Reversible gate is NOT gate and is a  $1*1$  gate. Quantum cost of NOT gate is zero.

(a) Input(A) Output(P)

1 0

0 1

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2) CNOT GATE CNOT gate is also known as controlled-not gate. It is a  $2 \times 2$  reversible gate. Quantum cost of CNOT gate is 1.

(a) A B P Q

0 0 0 0

0 1 0 1

1 0 1 1

1 1 1 0

3) FEYNMAN Gate The Feynman gate is a  $2 \times 2$  gate and is also called as Controlled NOT gate. Quantum cost of Feynman gate is 1.

(a) A B P Q

0 0 0 0

0 1 0 1

1 0 1 1

1 1 1 0

4) FREDKIN GATE Fredkin gate is  $3 \times 3$  gates. It is a universal gate .Quantum cost of Fredkin gate is 5.

(a) A B C P Q R

0 0 0 0 0 0

0 0 1 0 0 1

0 1 0 0 1 0

0 1 1 0 1 1

1 0 0 0 0 0

1 0 1 1 1 0

1 1 0 1 0 1

1 1 1 1 1 1

4) TOFFOLI Gate Toffoli gate is a  $3 \times 3$  gate. It is also a universal gate. Quantum cost of Toffoli gate is 5.

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A B C P Q R

0 0 0 0 0

0 0 1 0 0 1

0 1 0 0 1 0

0 1 1 0 1 1

1 0 0 0 0 0

1 0 1 1 0 1

1 1 0 1 1 1

1 1 1 1 1 0

In 2010, Lihui Ni et.al [3] presented a general method of constructing the reversible full adder. A range of reversible full adders with only two reversible gates and two garbage outputs were realized using this approach. This approach had progress in the gate count, garbage count and quantum cost.

In 2011, Nagapavani et.al [4] presented a paper that proposed a design of a reversible 4-bit shift registers which were compared with previous design. For this proposed designs Reversible edge triggered D flip-flop such as SISO, SIPO, PISO and PIPO. These designs have the applications to perform serial-to-parallel and parallel-to-serial conversions.

In 2011, Zhijin Guan et.al [5] presented a design of Arithmetic Logic Unit based on reversible logic gates. This paper presents that the minimum number of information bits were required for designing reversible Arithmetic Logic Unit. This design has low power consumption and reduces the loss by reusing information bits.

In 2012, T. Naga Babu et.al [6] presented reversible adder/subtractor circuits using reversible logic gates like DKG and TSG gate. The proposed designs were better than the previous designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs.

In 2012, Xueyun Cheng et.al [7] presented a simplification algorithm for reversible logic networks of positive/ negative control gates. This algorithm can lessen the gate count as well as number of control bits. This simplified algorithm required only 8.10 average numbers of control bits and 11 gate counts.

In 2013 Rakshith Saligram et.al [8] presented a design of low logical cost adders using novel parity conserving Toffoli gate. In this design parity preserving gate had itself been used to work as a Toffoli gate. This proposed design has a slightest logical cost. This design has 22.22% enhancement for quantum cost.

In 2013, Mr. M.Saravanan et.al [9] presented a design of energy efficient code converters using

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reversible logic gates. This paper describes the various code converters such as grey to binary, binary to grey, BCD to excess-3 using reversible logic gates. These converters have low power consumption and higher efficiency as compared with conventional logic circuits.

In 2014, Avinash G.Keskar et.al [10] presented a design of eight bit novel reversible arithmetic and logic unit. This design can be used to realize large reversible systems. A reversible implementation of eight bit arithmetic and logic unit required less number of gates and garbage outputs. In 2014, R.Jayashree et.al [11] proposed that flip flops such as D flip-flop, T flip-flop and JK flip-flop were designed using various previous reversible gates and their truth table were verified by simulation. These proposed designs were compared in terms of average power consumption, garbage outputs and constant inputs.

In 2014, Asima Jamal et.al [12] proposed a design of sixteen bit binary sequential counter using Feynman and Fredkin gates. The Up/Down operation of this design was controlled by the control input UP/DOWN. The control input should be 1 for UP operation and the control input should be 0 for down operation.

In 2014, Ankur Sarker et.al [13] presented a design that performs addition/ subtraction operations using parity preserving and fault tolerant reversible gates. This circuit not only reduced the number of logic gates but also reduced the quantum cost and garbage outputs. The highest improvements of the presented design were 33.33% for garbage output, 26.66% for quantum cost and 50% for gate count.

In 2015, Sayyad khaja Moinuddin et.al [14] proposed 2:4 reversible decoder using two Feynman and two Fredkin gates. The proposed reversible decoder can be used in active high as well as in active low mode of operation which depends upon the select lines. The proposed design has low quantum cost and this design can be extended to 3:8 decoders.

In 2015, Md. Samiur Rahman et.al [15] proposed an Optimized Design of Full-Subtractor Using New SRG Reversible Logic Gates and VHDL Simulation. In this proposed design SRG gate worked singly as a Full-subtractor circuit. This proposed work can be used for designing nanotechnology based large reversible systems.

In 2015, Avishek Bose et.al [16] presented a design of compact reversible online testable ripple carry adder. The main property of this design is that one input line of the adder has no control on the other input line. This design has improvement of 25% on number of gates, 42.30% on quantum cost and 50% on number of constant inputs.

In 2016, Umesh Kumar et.al [17] proposed a paper that describes the performance evaluation of reversible logic gates. In this paper classical gates and quantum gates are compared on the various parameters. It is analyzed that power consumption, heat dissipation can be minimized using various reversible logic gates such as Toffoli, Fredkin and Peres gate.

In 2016, Deeptha A et.al [18] proposed a design of Reversible 8-bit ALU by cascading 1-bit ALUs. Control unit and the adder unit were the major units of 1-bit ALUs. Control Output Gate (COG) and Haghparast Navi Gate (HNG) have been used for control unit and adder unit respectively. The proposed design was compared with the previous design and has lesser propagation delay.

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In 2016, MojtabaValinataj et.al [19] proposed a design of a new low-cost gate with the quantum cost of 10. This new low-cost gate was used as a parity preserving full adder with the minimum hardware complexity. Some new low-cost fault-tolerant adders are carry skip, carry look-ahead and BCD adders which are highly proficient in terms of quantum cost, total logical calculation and transistor count as compared to the previous designs

In 2017, A.V.Ananthalakshmi et.al [20] proposed a design of Reversible floating-point square root using modified non-restoring algorithm. Non-restoring method consumed less number of logical resources and the remainder was not restored in each step. GST algorithm was used for this floating-point square root which has reduced the area and power consumption. This design is efficient in terms of number of reversible gates, constant inputs, garbage outputs and quantum cost.

In 2017, A.Kamaraj et.al [21] presented a design of Arithmetic Logic Unit using Novel reversible gates and it was evaluated in Quantum Cellular Automata. This Arithmetic Logic Unit can be used for low power applications. This design mitigates quantum cost, garbage outputs. It has improvement of 50% on constant inputs, 58.3% on gate counts and 62% on number of cells.

In 2017, Dhoumendra Mandal et.al [22] presented a design of all optical one bit binary comparator using reversible logic gates. In this design, reversible logic gates based on frequency encoded data were used for designing one bit comparator. This comparator circuit can be used to propose all optical Arithmetic Logic Unit.

In this research, we reviewed different papers in which proposed designs are compared with the previous designs. The proposed designs make use of different reversible gates such as Feynman gate, fredkin gate, toffoli gate, SRG gate, LCG gate etc. These reversible logic gates makes them better than the previous designs in terms of quantum cost, number of garbage outputs, constant inputs and power consumption. These designs can be used in quantum computing and nanotechnology.